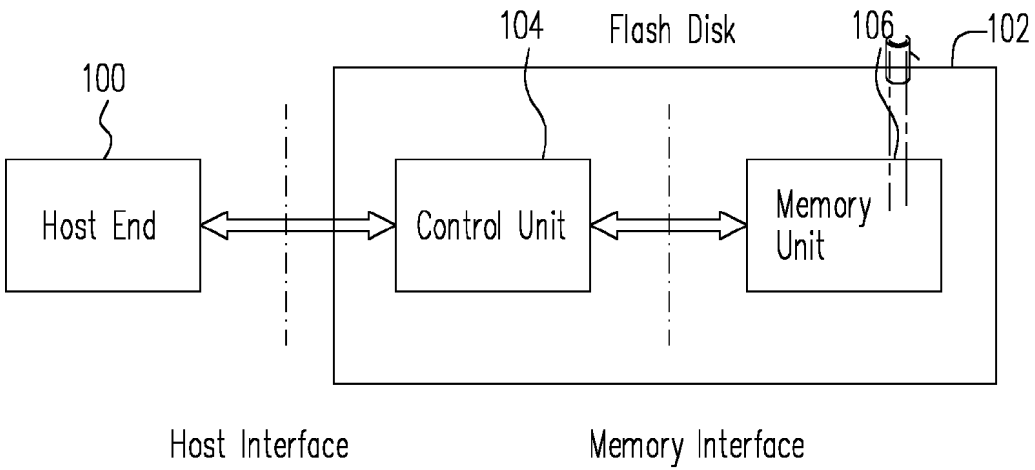



FIG. 1 (PRIOR ART)

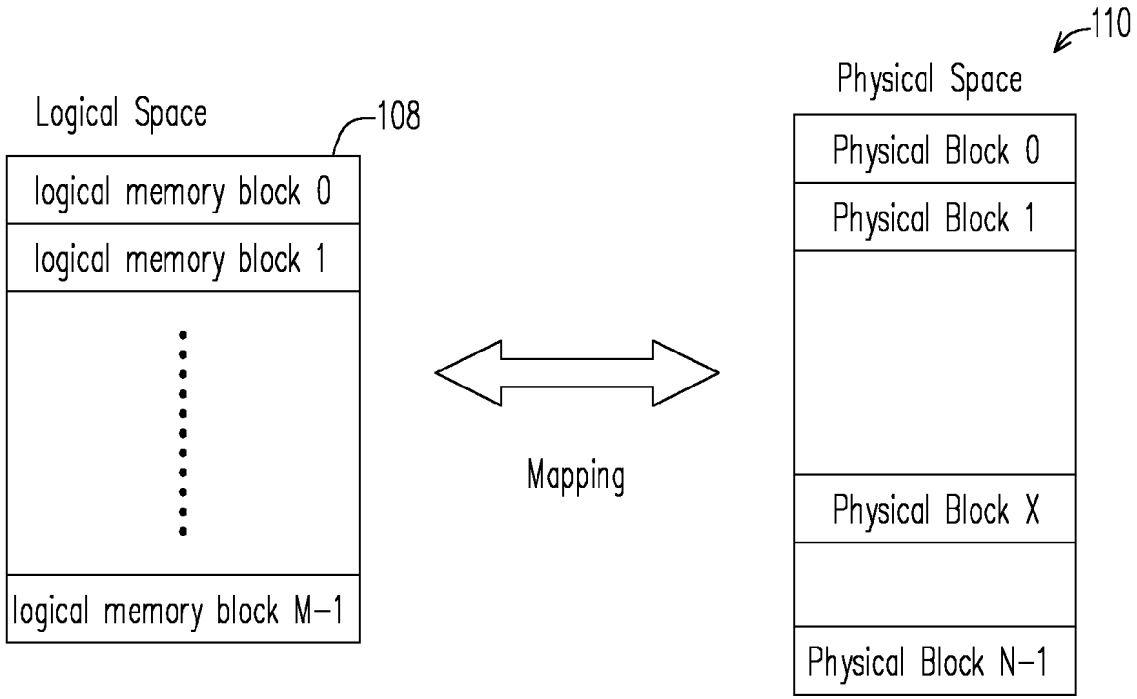



FIG. 2 (PRIOR ART)

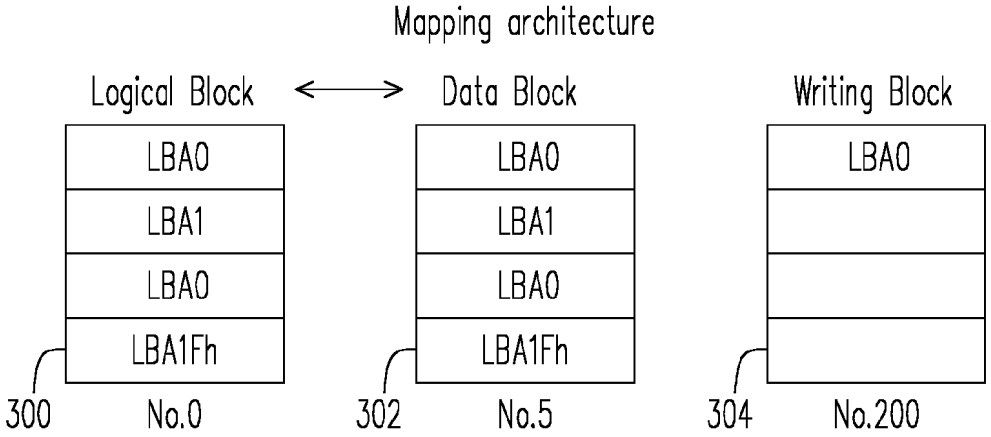



FIG. 3A(PRIOR ART)

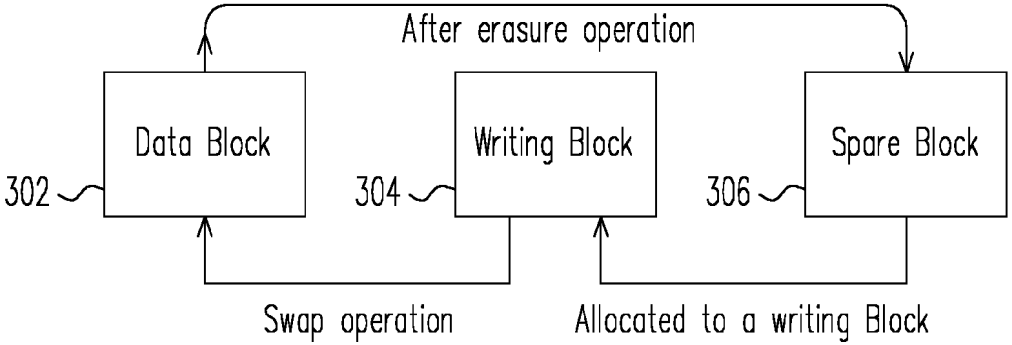



FIG. 3B(PRIOR ART)

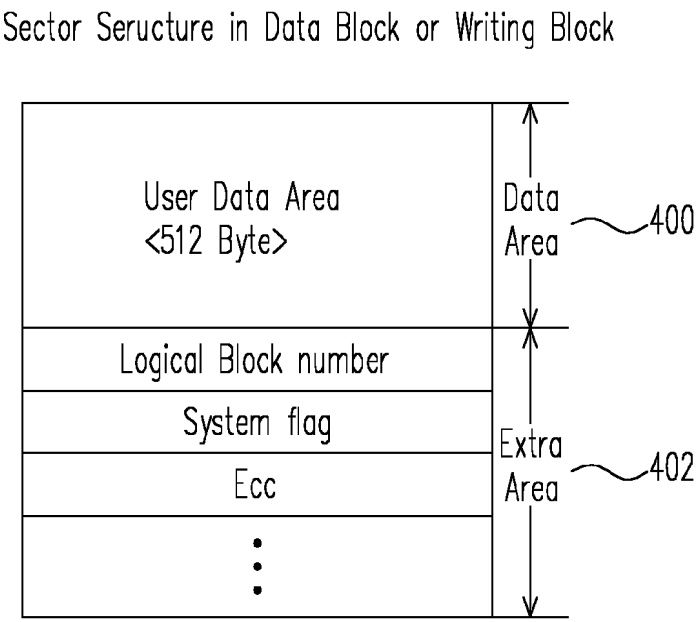
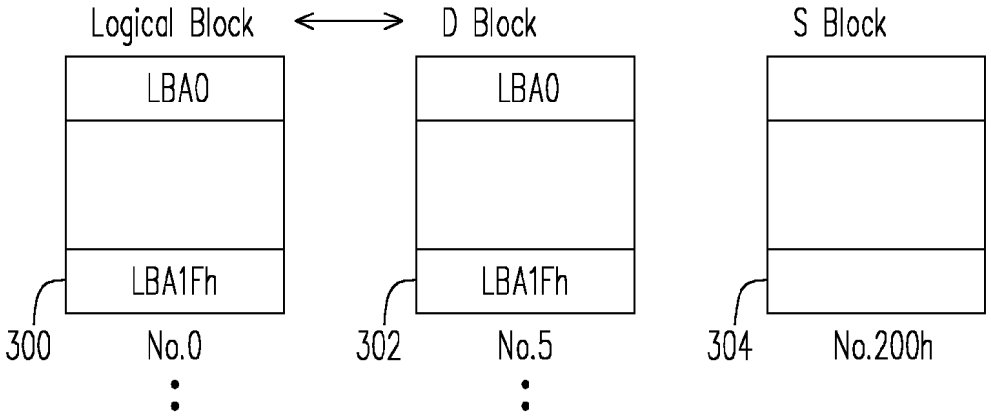


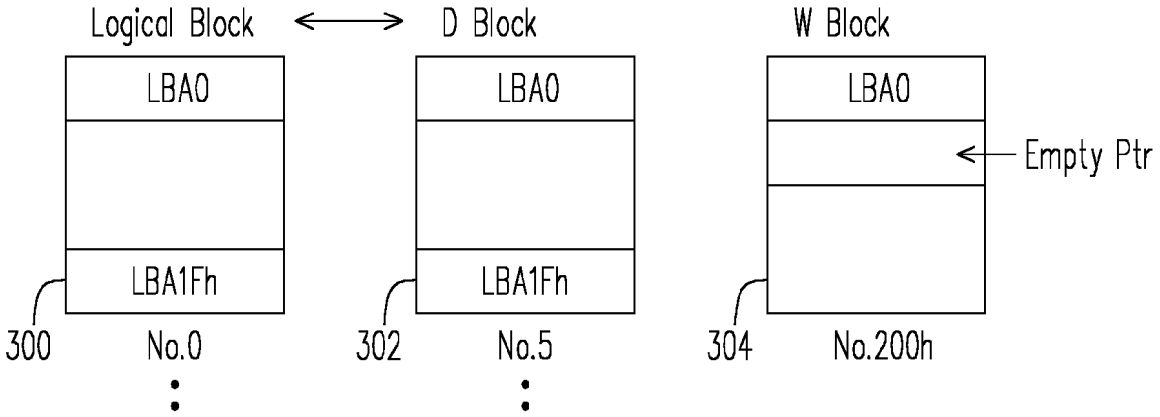

FIG. 4 (PRIOR ART)




Logical ⟷ physical

| Logical Block No. | Data Block No. | W(S) Block No. | Empty Ptr | Other status |
|---|---|---|---|---|
| 0 | 5 | 200h | FFFFh | ••••• |
| 1 | 9 | | | |
| ⋮ | ⋮ | | | |
| | | | | |
| ⋮ | ⋮ | | | |

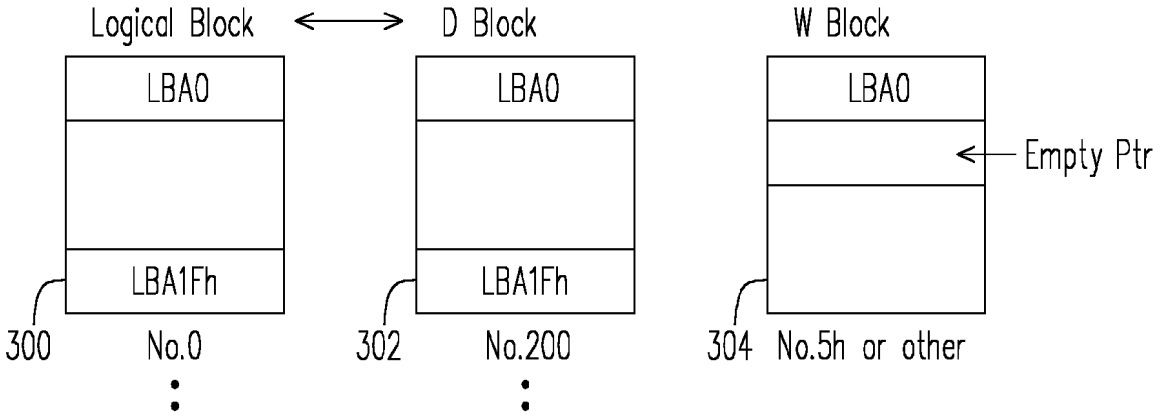
FIG. 5 (PRIOR ART)




Logical ⟷ physical

| Logical Block No. | Data Block No. | W(S) Block No. | Empty Ptr | Other status |
|---|---|---|---|---|
| 0 | 5 | 200h | 1 | ..... |
| 1 | 9 | | | |
| ⋮ | ⋮ | | | |
| | | | | |
| ⋮ | ⋮ | | | |

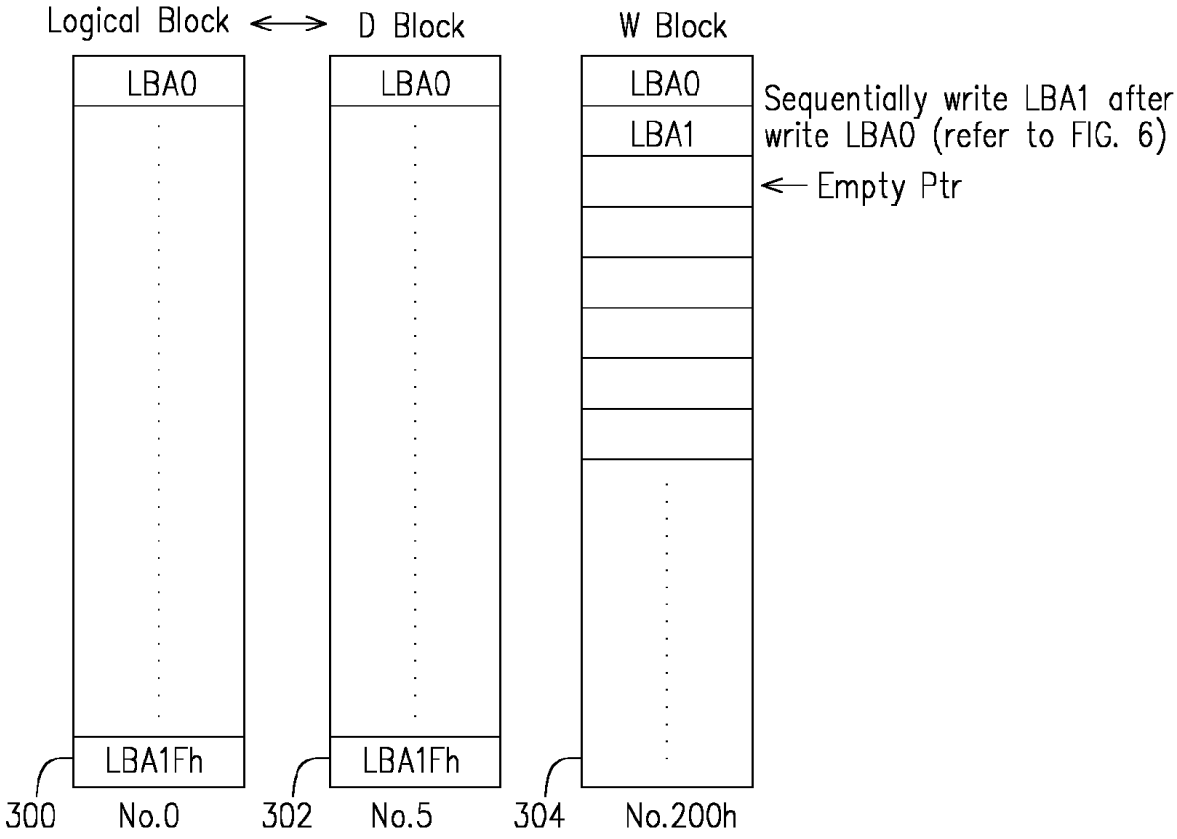
FIG. 6 (PRIOR ART)




Logical ⟷ physical

| Logical Block No. | Data Block No. | W(S) Block No. | Empty Ptr | Other status |
|---|---|---|---|---|
| 0 | 200 | 5h or other | 1 | ••••• |
| 1 | 9 | | | |
| ⋮ | ⋮ | | | |
| | | | | |
| ⋮ | ⋮ | | | |

FIG. 7 (PRIOR ART)




Logical ⟷ physical

| Logical Block No. | Data Block No. | W(S) Block No. | Empty Ptr | Other status |
|---|---|---|---|---|
| 0 | 5 | 200h | 2 | ⋮ |
| 1 | 9 | | | |
| ⋮ | ⋮ | | | |

FIG. 8 (PRIOR ART)

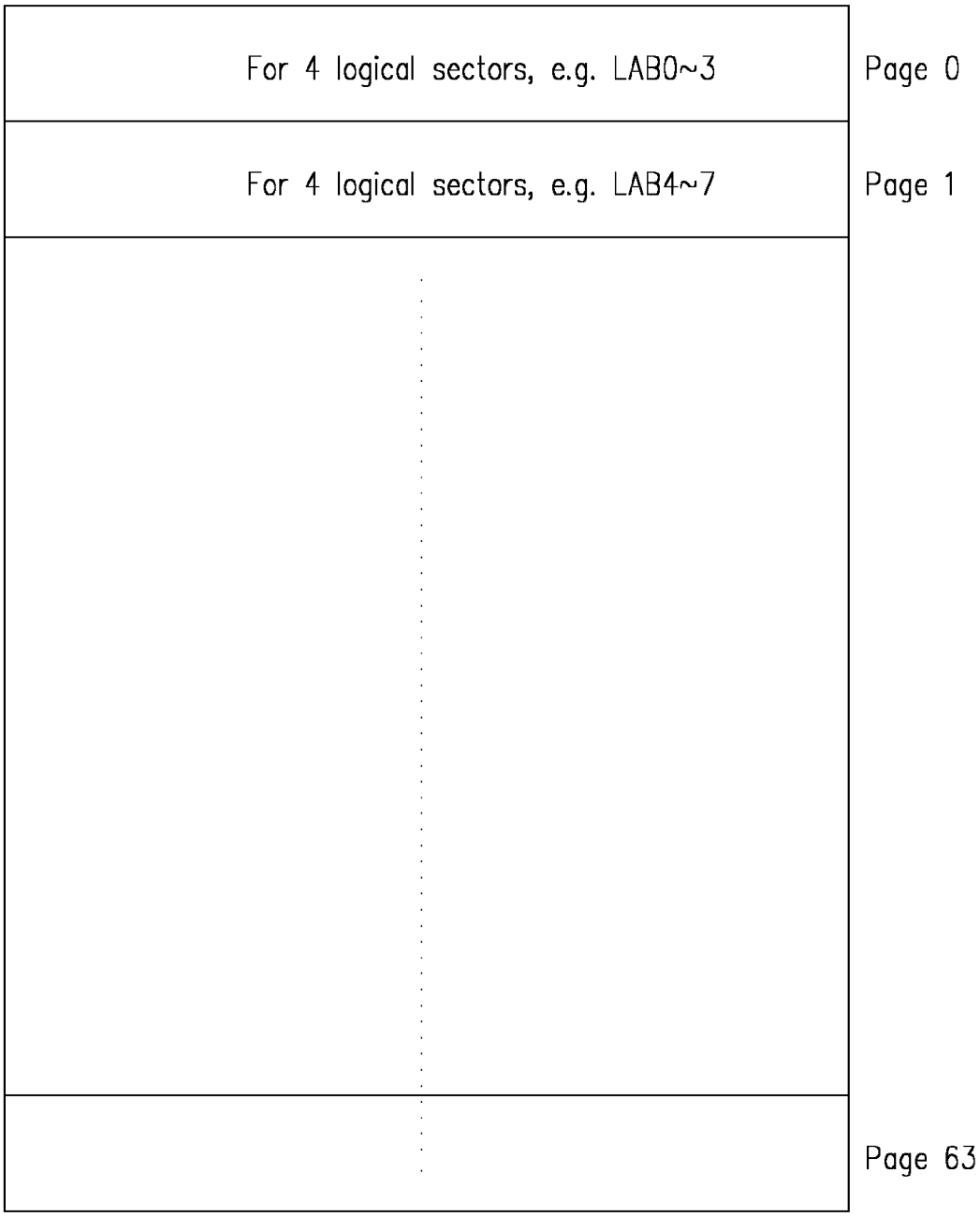
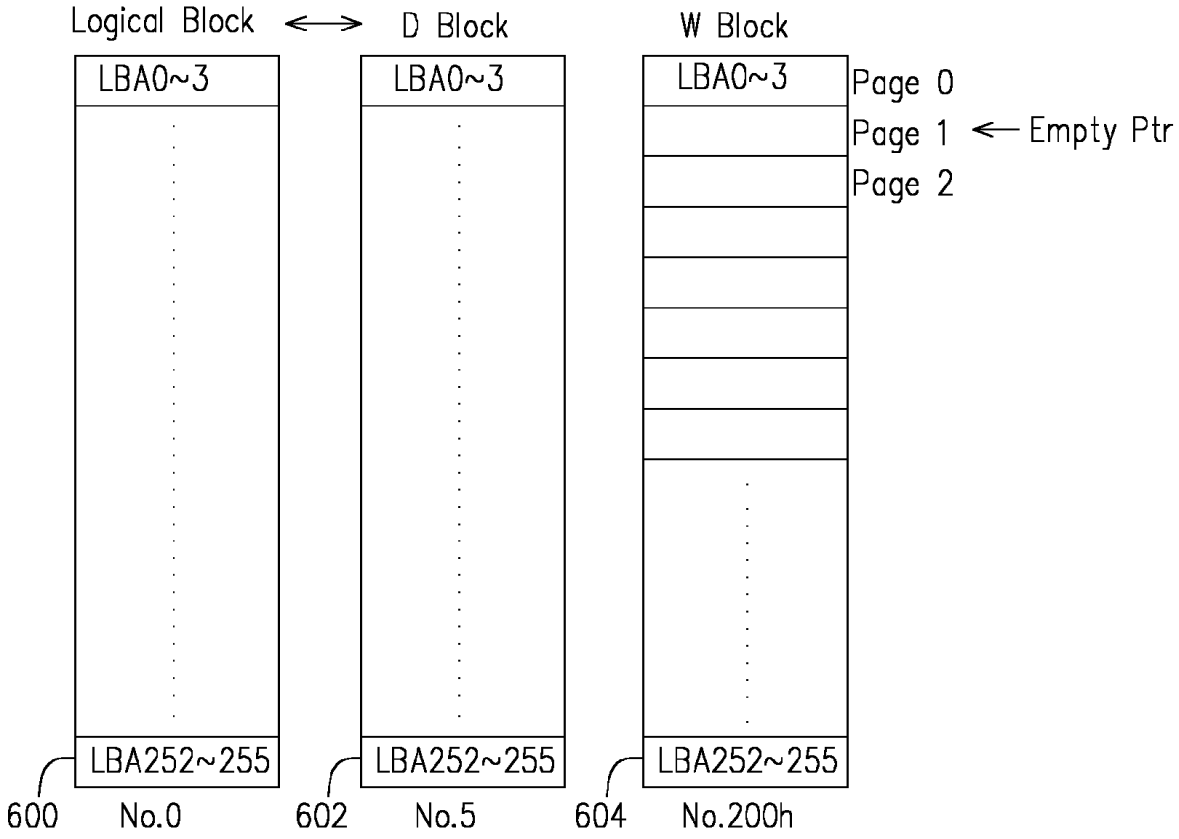


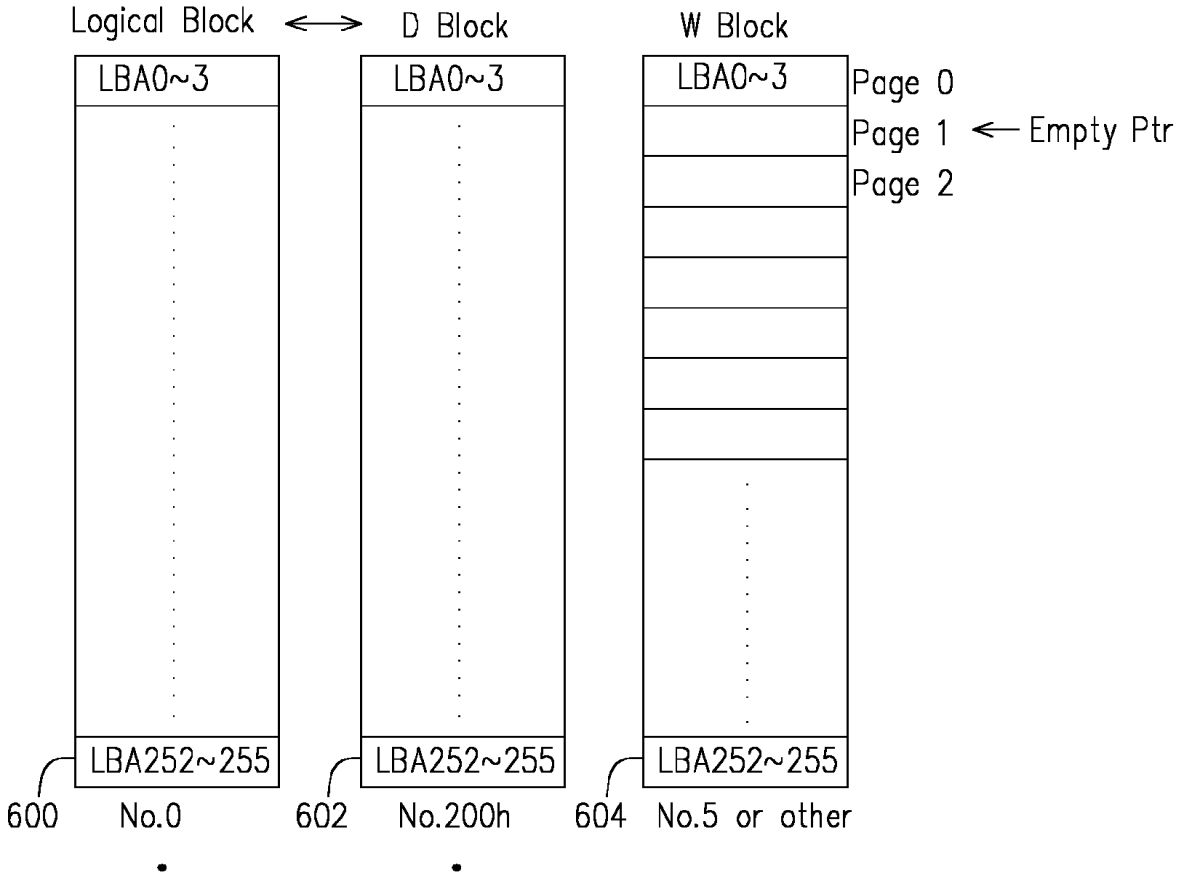

FIG. 9 (PRIOR ART)




Logical ⟷ physical

| Logical Block No. | Data Block No. | W(S) Block No. | Empty Ptr | Other status |
|---|---|---|---|---|
| 0 | 5 | 200h | 1 | ⋮ |
| 1 | 9 | | | |
| ⋮ | ⋮ | | | |

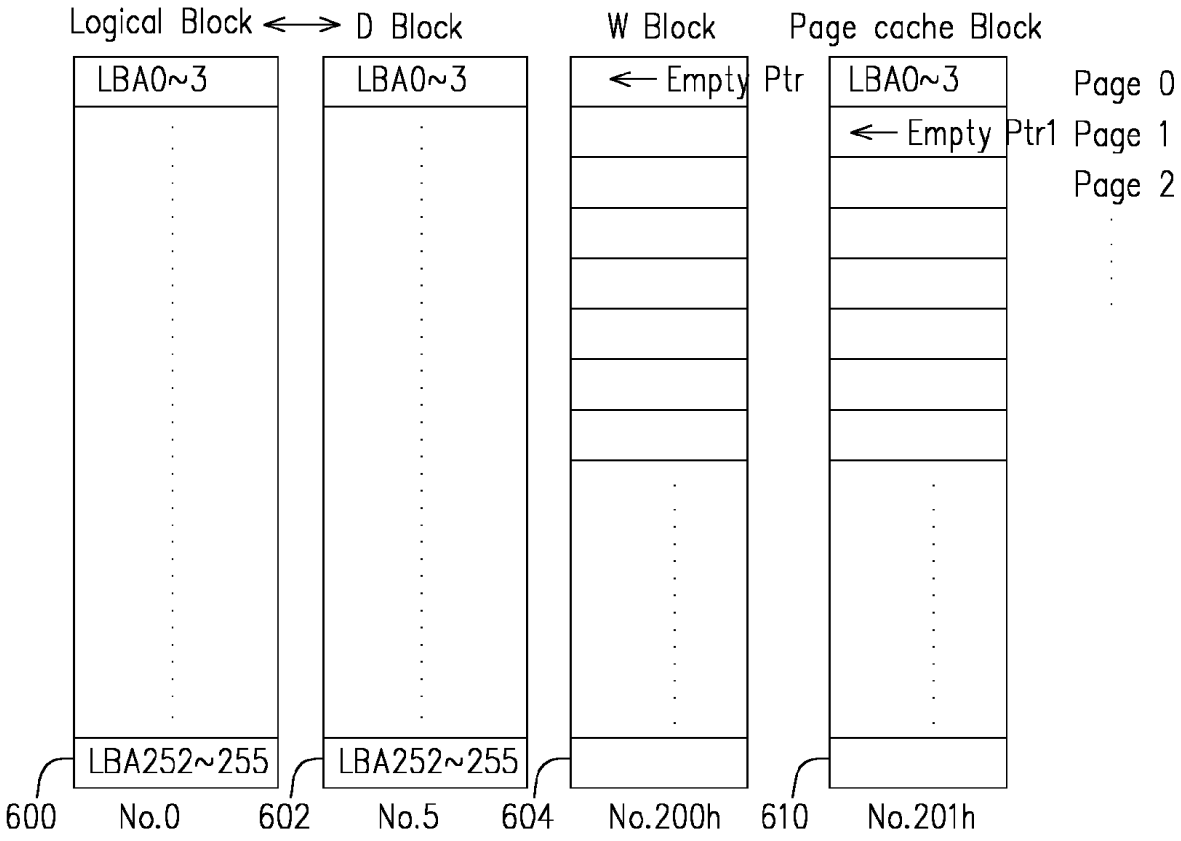
FIG. 10(PRIOR ART)




Logical ⟷ physical

| Logical Block No. | Data Block No. | W(S) Block No. | Empty Ptr | Other status |
|---|---|---|---|---|
| 0 | 200h | 5 or other | 1 | |
| 1 | 9 | | | |
| | | | | |

FIG. 11(PRIOR ART)



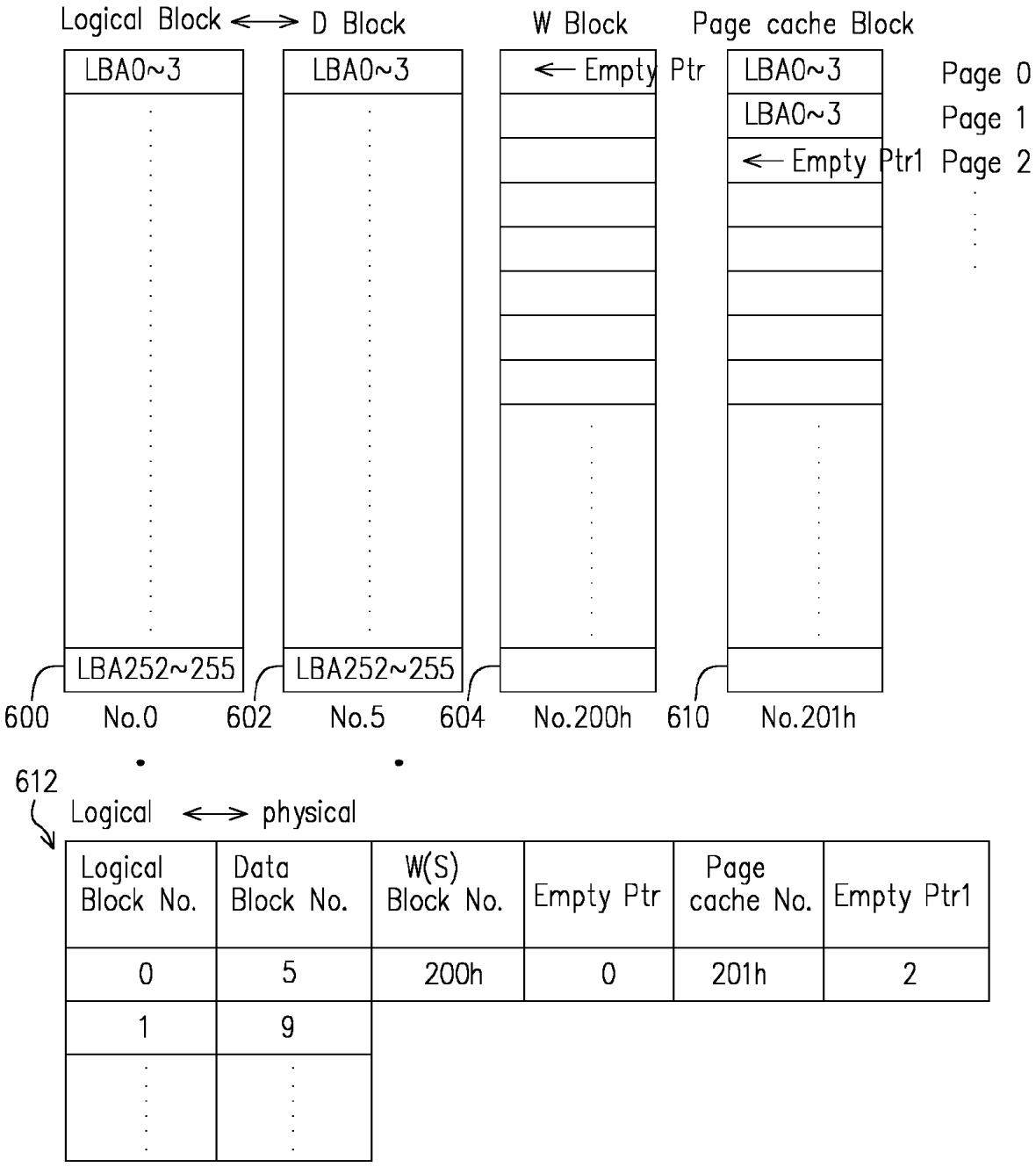

612 Logical ⟷ physical

| Logical Block No. | Data Block No. | W(S) Block No. | Empty Ptr | Page cache No. | Empty Ptr1 |
|---|---|---|---|---|---|
| 0 | 5 | 200h | 0 | 201h | 1 |
| 1 | 9 | | | | |
| | | | | | |

614

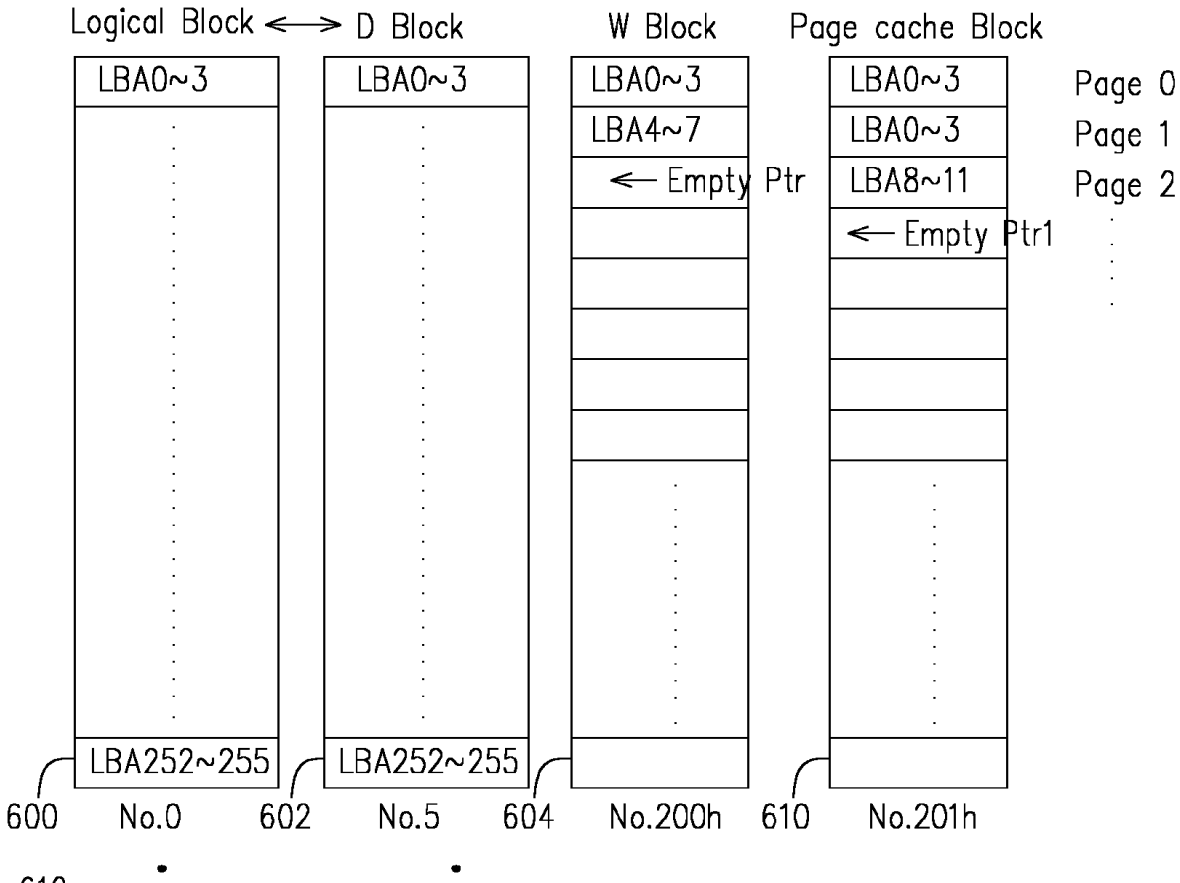
616

FIG. 12




| Logical Block No. | Data Block No. | W(S) Block No. | Empty Ptr | Page cache No. | Empty Ptr1 |
|---|---|---|---|---|---|
| 0 | 5 | 200h | 0 | 201h | 2 |
| 1 | 9 | | | | |
| ⋮ | ⋮ | | | | |

FIG. 13




612

Logical ⟷ physical

| Logical Block No. | Data Block No. | W(S) Block No. | Empty Ptr | Page cache No. | Empty Ptr1 |
|---|---|---|---|---|---|
| 0 | 5 | 200h | 2 | 201h | 3 |
| 1 | 9 | | | | |
| ⋮ | ⋮ | | | | |

FIG. 14

| | Step 1 | Step 2 | Step 3 |
|---|---|---|---|
| Host behavior | Write LBA0,SC=1<br>Write LBA0,SC=1 | Sequentially write LBA1,SC=1 | Random write LBA0,SC=10 |
| Controller behavior based on prior algorithm | Write page0 of W block | Overwrite page0 Need swap operation | Overwrite page0 Need swap operation |
| Controller behavior based on this invention | Write page0 of page cache block | Write page1 of page cache block | Write page0~1 of W block and then write page 2 of page cache |

FIG. 15

Sector (512+16B) structure of a page (2048+64B) in a page cache block

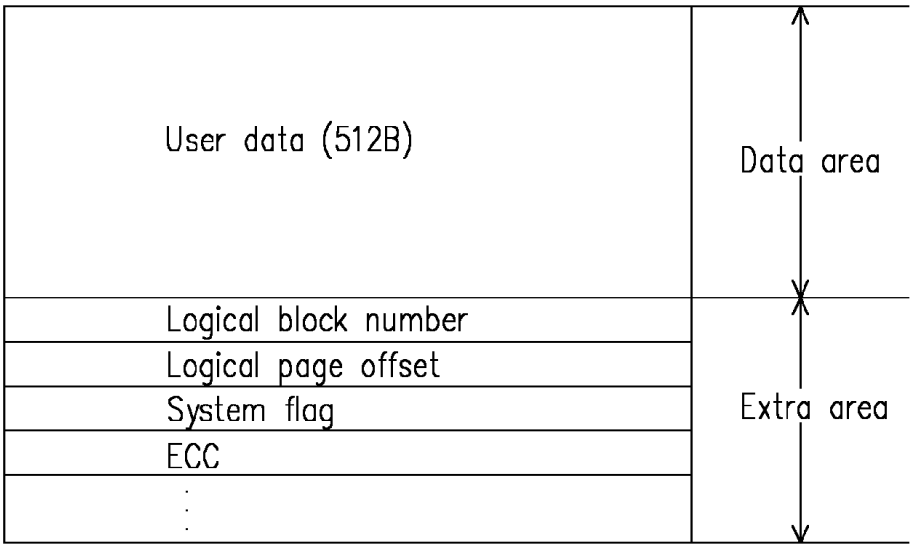



FIG. 16